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10EC009

M.Tech. Degree Examination, December 2011
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Describe the structure, operation and current-voltage characteristics of a MESFET. Also mention the applications of MESFETs. **(10 Marks)**

b. What is modulation doping? How is it done? Explain with the help of band diagram. Hence describe the structure of a MODFET. **(10 Marks)**

2 a. Describe a typical Management Information System structure. Also describe the energy band diagram for an ideal n-type Management Information System structure biased in accumulation, depletion and inversion. **(12 Marks)**

b. Describe the small signal model for a MOSFET. Also calculate the transconductance of a MOSFET, given that L = 5 μm, z = 50 μm, $V_G = 2$ V, $V_{threshold} = 0.98$ V, $\mu_n' = 500$ cm/vs, $C_i = 115$ nF/cm^2. **(08 Marks)**

3 a. Explain with suitable diagrams, short channel effects on threshold voltage and surface mobility in a MOSFET. **(10 Marks)**

b. Explain the processing challenges to CMOS miniaturization. **(10 Marks)**

4 a. Explain the energy level diagram for a molecular diode under equilibrium, forward and reverse bias. **(10 Marks)**

b. Describe a nanoFET device. Also list advantages and disadvantages of carbon nano tubes. **(10 Marks)**

5 a. What is the need for super buffers? Explain NMOS inverting and non-inverting super buffers with the help of schematic and stick diagrams. **(10 Marks)**

b. Describe the salient features of pass transistor logic design. Hence design 2 variables (A, B) pass transistor structure for, i) 1-bit multiplier ii) 1-bit 1's complement. **(10 Marks)**

6 a. Explain the sum of products (SOP) and ROM look-up table implementation of a 3 input tally circuit. Also draw the stick diagram for a 3-input tally circuit using pass transistors. Explain the operation in the form of a table and list the salient features of the same. **(10 Marks)**

b. Design a dynamic CMOS NAND-NAND logic for a circuit whose output F7B is defined by, $F7B = \sum_{xyz}(1, 3, 5, 7)$

Assume that $X, \overline{X}, Y, \overline{Y}, Z$ and $\overline{Z}$ are readily available. Draw the stick diagram for F7B. **(10 Marks)**

7 a. Write the salient features of a barrel shifter. Design a 4-bit programmable barrel shifter. What is the propagation delay and regularity of this circuit? **(10 Marks)**

b. With a suitable example, describe Lee-Moore maze search algorithm for local routing. Also suggest a scheme to reduce the associated computation time. **(10 Marks)**

8 Write short notes on the following:

a. Hierarchy and regularity in IC design.

b. Design using programmable logic structures.

c. Programmable interconnects.

d. Standard cell design. **(20 Marks)**

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